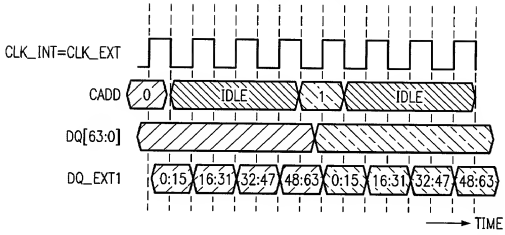
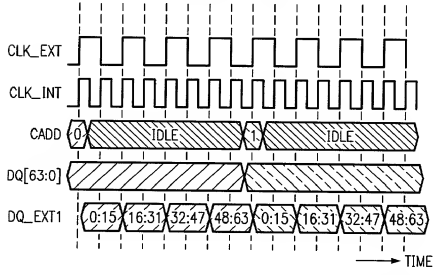
FIG. 1
(PRIOR ART)



Data read sequence for a 64 bit data bus and a 16 bit wide external tester interface (internal clock frequency= external clock frequency). Note that between each read operation the eDRAM will stay for 3 cycles in idle mode.

FIG. 2
(PRIOR ART)



Data read sequence for a 64 bit data bus and a 16 bit wide external tester interface (internal clock frequency= 2x external clock frequency). Note that between each read operation the eDRAM will stay for 7 cycles in idle mode.

FIG. 3

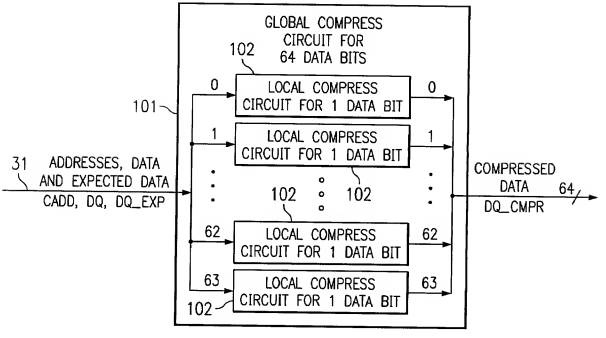

GLOBAL COMPRESS CIRCUIT FOR 64 DATA BITS
102
101
0
LOCAL COMPRESS CIRCUIT FOR 1 DATA BIT
0
1
LOCAL COMPRESS CIRCUIT FOR 1 DATA BIT
1
31
ADDRESSES, DATA AND EXPECTED DATA
CADD, DQ, DQ_EXP
102
102
COMPRESSED DATA
64
DQ_CMPR
62
LOCAL COMPRESS CIRCUIT FOR 1 DATA BIT
62
63
LOCAL COMPRESS CIRCUIT FOR 1 DATA BIT
63
102

FIG. 6

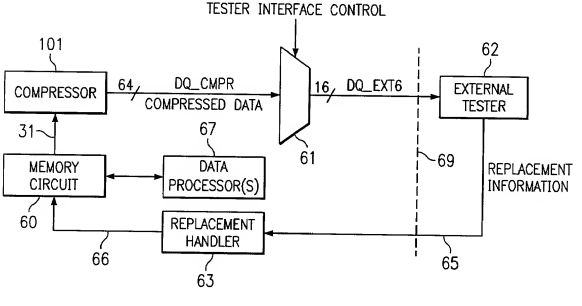

TESTER INTERFACE CONTROL
101
COMPRESSOR
64
DQ_CMPR
COMPRESSED DATA
16
DQ_EXT6
62
EXTERNAL TESTER
31
67
61
69
REPLACEMENT INFORMATION
MEMORY CIRCUIT
DATA PROCESSOR(S)
60
REPLACEMENT HANDLER
66
63
65

FIG. 4

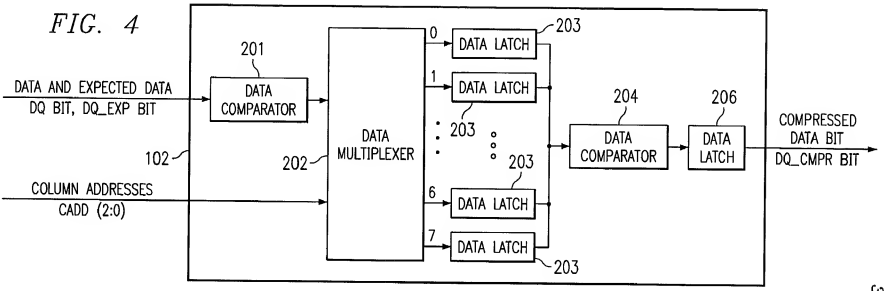
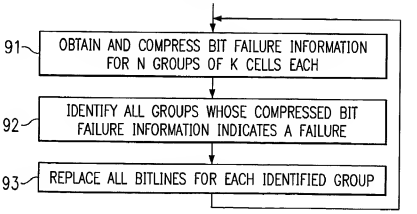

201
DATA AND EXPECTED DATA
DQ BIT, DQ_EXP BIT
DATA COMPARATOR
102
202
COLUMN ADDRESSES
CADD (2:0)
DATA MULTIPLEXER
0
1
6
7
DATA LATCH
203
204
DATA COMPARATOR
206
DATA LATCH
COMPRESSED DATA BIT
DQ_CMPR BIT

FIG. 9


91
OBTAIN AND COMPRESS BIT FAILURE INFORMATION FOR N GROUPS OF K CELLS EACH
92
IDENTIFY ALL GROUPS WHOSE COMPRESSED BIT FAILURE INFORMATION INDICATES A FAILURE
93
REPLACE ALL BITLINES FOR EACH IDENTIFIED GROUP

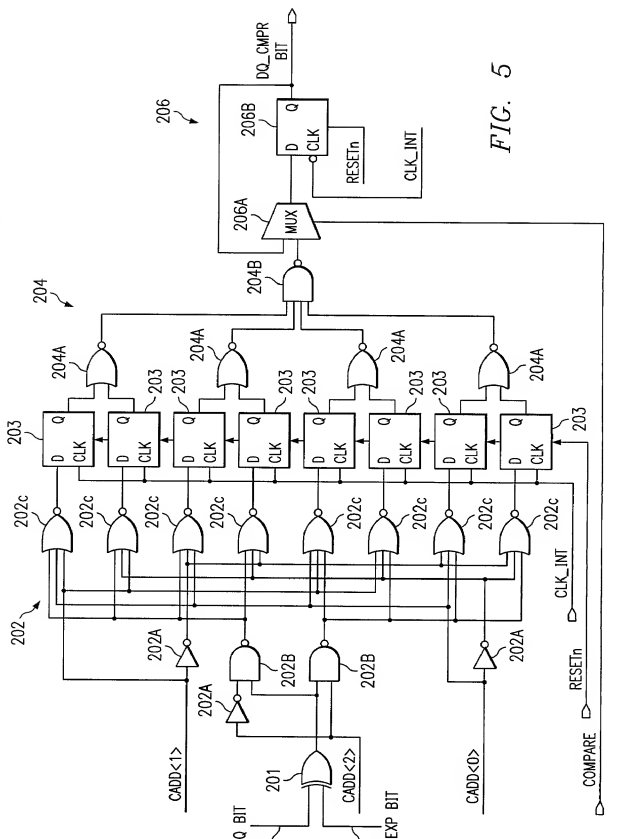
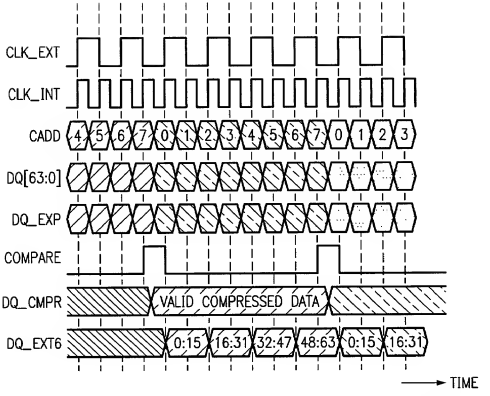

DQ_CMPR BIT
206
206B
D
Q
CLK
RESETn
CLK_INT
206A
MUX
204B
204
204A
203
202c
202
202A
202B
CADD<1>
CADD<2>
CADD<0>
201
DQ BIT
51
52
DQ_EXP BIT
CLK_INT
RESETn
COMPARE

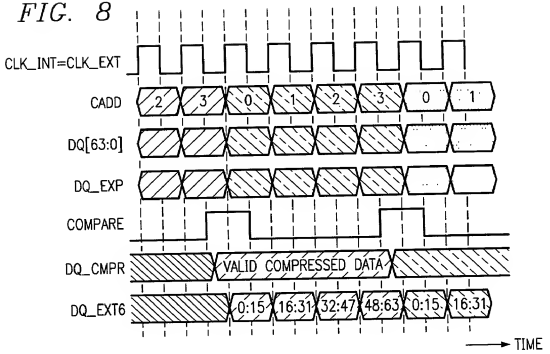
FIG. 5

FIG. 7



Data read sequence for a 64 bit data bus and a 16 bit wide external tester interface (internal clock frequency=2x external clock frequency). Note that the time for multiplexing the compressed data (from previous read cycles) to the tester is used to compress the current read data. No cycles are lost, 8 bit compression.

FIG. 8



Data read sequence for a 64 bit data bus and a 16 bit wide external tester interface (internal clock frequency=external clock frequency). Note that the time for multiplexing the compressed data (from previous read cycles) to the tester is used to compress current read data. No cycles are lost, 4 bit compression.